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[Title of the Invention] Magnetic Memory And Driving Method Therefor

[What is Claimed is]

[Claim 1]

A magnetic memory comprising:

a plurality of variable resistors arrayed as memory elements in a matrix;

a plurality of bit lines each of which is arranged on each row of the matrix and connected to one terminal of each variable resistors belonging to the same row;

a read circuit which detects resistance values of said variable resistors based on currents flowing through said bit lines; and

a load element arranged on said bit lines independently of said memory elements.

[Claim 2]

A memory according to claim 1, wherein said load element is to suppress a fluctuation of a load of said bit line.

[Claim 3]

A memory according to claim 1, wherein said load element includes a resistor having the same structure as a structure of said variable resistor, a resistor having a structure different from the structure of said variable resistor, a current source, a diode, or a combination of the resistor, the current source, and the diode.

[Claim 4]

A memory according to claim 1, wherein each variable resistor includes a tunneling magnetoresistive element.

[Claim 5]

A memory according to claim 4, wherein said tunneling magnetoresistive element is magnetized mainly perpendicular to a film surface.

[Claim 6]

A memory according to claim 4, wherein said tunneling magnetoresistive element is magnetized mainly parallel to a film surface.

[Claim 7]

A memory according to claim 1, further comprising a plurality of switches for selecting said variable resistors in correspondence with said variable resistors.

[Claim 8]

A memory according to claim 7, wherein each switch includes a field effect type transistor, a bipolar transistor, a thin film transistor, a diode, or a combination of the field effect type transistor, the bipolar transistor, the thin film transistor, and the diode.

[Claim 9]

A ferromagnetic memory driving method for driving a memory as defined in Claim 1, comprising the steps of:

selecting said variable resistors connected to the same bit line continuously so as to apply a predetermined voltage to said variable resistors; and

detecting information written in the variable resistors based on currents flowing through the variable resistors.

[Claim 10]

A ferromagnetic memory driving method according to Claim 9, comprising the steps of:

selecting said variable resistors connected to the same bit line continuously and suppressing variations in the voltages of the bit lines including said variable resistors when applying a predetermined voltage to said variable resistors.

[Claim 11]

A ferromagnetic memory driving method according to claim 10, wherein the step of suppressing variations in the voltages of the bit lines is a step of always turning on one of the plurality of switches connected to the same bit line.

[Claim 12]

A ferromagnetic memory driving method for driving a nonvolatile memory which comprises a plurality of variable resistors arranged in a matrix, a plurality of switches respectively corresponding to said variable resistors, and a plurality of bit lines arranged on each row of the matrix, one terminal of each variable resistor being connected to the same bit line and the other terminal of said variable resistor being connected to one terminal of each corresponding switch,

said driving method comprising the steps of:

suppressing variations in the voltages of said bit line including said variable resistors to apply a predetermined voltage to said variable resistor; and

detecting information written in the variable resistors based on currents flowing through the variable resistors.

[Claim 13]

A ferromagnetic memory driving method according to claim 12, wherein the step of suppressing variations in the voltages of the bit lines is a step of always turning on one of the plurality of switches connected to the same bit line.

[Claim 14]

A method for driving a ferromagnetic memory which comprises a plurality of variable resistors arranged in a matrix and capable of selecting an electric resistance by selecting a direction of magnetization of a ferromagnet, a plurality of switches respectively corresponding to said variable resistors, and a plurality of bit lines arranged on each row of said matrix, one terminal of each variable resistor being connected to the same bit line and the other terminal of said variable resistor being connected to one terminal of each corresponding switch, said driving method comprising the step of:

selecting two or more of said plurality of variable resistors connected to the same bit line continuously so as to always select at least one of said variable resistors connected to the same bit line when reading information.

[Detailed Description of the Invention]

[0001]

[Field of the Industrial Utilization]

The present invention relates to a memory for storing information, and, more particularly, to a nonvolatile memory using a ferromagnet and a driving method therefor.

[0002]

[Prior Art]

In general, a ferromagnet has a property that magnetization generated within the ferromagnet by an externally applied magnetic field remains even after removal of the external magnetic field (this is called residual magnetization). The resistance of the ferromagnet changes depending on the magnetization direction, the presence/absence of magnetization, or the like. This is called a magnetoresistance effect. The change ratio of the resistance is called a MR ratio (MagnetoResistance ratio). Materials having high MR ratios are a GMR (Giant MagnetoResistance) material and a CMR (Colossal MagnetoResistance) material. These materials consist of metals, alloys, composite oxides, and the like. Examples of these materials are transition metals and rare earth metals such as Fe, Ni, Co, Gd, and Tb, alloys of them, and composite oxides such as $La_xSr_{1-x}MnO_9$ and $La_xCa_{1-x}MnO_9$. A nonvolatile memory for storing information by selecting the resistance depending on the difference in magnetization direction or the presence/absence of magnetization by utilizing the residual magnetization of such a magnetoresistance material can be constituted. This nonvolatile memory is called an MRAM (Magnetic Random Access Memory).

[0003]

Most of MRAMs which have recently been developed adopt the following method. That is, ferromagnetic memory cells for storing information by residual magnetization of the ferromagnet of a giant magnetoresistance material are formed. A change in resistance by the difference in magnetization direction is converted into a voltage to read out stored information. In addition, the magnetization direction of a ferromagnetic memory cell is changed by a magnetic field induced by flowing a current through a write wire, and information can be written in the memory cell or rewritten.

[0004]

The cell structure and driving method of an MRAM are described in R. E. Scheuerlein (1998, Proc. of Int NonVolatile Memory Conf. p. 47).

[0005]

This reference proposes an MRAM in which a pair of write lines and a pair of read lines are laid out to cross each other, and an MRAM (matrix type) in which a pair of crossing wires serve as both write and read lines and which is made up of memory cells each containing a giant magnetoresistive thin film and diodes series-connected to the memory cells.

[0006]

These conventional MRAMs employ the following driving method. In reading out information from memory cells arrayed in a matrix, a bit line connected to a target memory cell is charged to a voltage level (to be referred to a target voltage Vt hereinafter) suitable for read operation. The target voltage Vt is applied across a variable resistor which constitutes the memory cell, thereby extracting a signal current flowing through the variable resistor.

[0007]

The bias voltage (target voltage Vt) dependency of the MR ratio reported in the materials (p. 15, Fig. 8) of the 117th Symposium (2000/12/22) of the Magnetics Society of Japan reveals that the MR ratio has a high bias dependency. For a high bias voltage, the MR ratio is difficult to maintain. In read operation of the MRAM, it is important to supply a target voltage Vt of about 100 to 300 mV with high precision.

[0008]

Fig. 10 is a circuit diagram for explaining read operation of a conventional MRAM. No selection switch is illustrated in Fig. 10 on the assumption that a memory cell subjected to read operation has already been selected.

[0009]

Referring to Fig. 10, only a variable resistor R and a field effect type transistor Tb for supplying the target voltage Vt are illustrated. In Fig. 10, the gate terminal of the field effect type transistor Tb receives a bias voltage Vb, and a source terminal voltage, i.e., target voltage Vt (= Vb - Vgs) is applied in accordance with a gate-source voltage Vgs.

[0010]

A signal current Isig flows through the variable resistor R in accordance with the target voltage Vt, and is transferred with a gain of 1 from the source terminal to drain terminal of the field effect type transistor Tb. More specifically, as shown in the signal current Isig - target voltage Vt characteristic of Fig. 11, the target voltage Vt is determined as a voltage value at an intersection point 113 between an I-V characteristic curve 111 of the variable resistor R and an I-V characteristic curve 112 of the field effect type transistor Tb.

[0011]

As is apparent from the graph of Fig. 11, the target voltage Vt cannot be maintained at a predetermined voltage upon large variations in the burden of the variable resistor

R connected as the load of the field effect type transistor Tb. In particular, the burden of a bit line in an indefinite state in which no connected memory cell is selected is greatly different from the burden exhibited when a memory cell is selected. Thus, the voltage level of the bit line is very different from the target voltage Vt.

[0012]

A conventional MRAM reading method is to read the information recorded by magnetization (magnetization information) by selecting an arbitrary memory cell at random. When no voltage is applied to the bit line, or when a selection switch of a memory cell connected to the bit line is not turned on, the voltage of the bit line is in an infinite state so that, whenever a memory cell is selected for reading the magnetization information, the bit line connected to the memory cell is charged to the target voltage Vt.

[0013]

[Problems to be Solved by the Invention]

For the conventional MRAM reading method, it is required, whenever selecting a memory cell for reading the magnetization information, to charge a bit line connected to the memory cell to the target voltage Vt. As a result, a high-speed reading of the magnetization information by MRAM is hindered by the time for charging the bit line.

[0014]

Fig. 12 is a timing charge for explaining an operation for reading information from an arbitrary memory cell continuously. Fig. 12 shows a voltage V_{BL} of the bit line BL, the signal current Isig, a load R_{BL} viewed from the bit line when the formation is read continuously from an arbitrary memory cell.

[0015]

A timing chart in Fig. 12 shows a state where, whenever any arbitrary bit line BL and memory are selected, the voltage V_{BL} of the bit line BL is charged to the target voltage Vt. From this timing chart, it can be understood that a certain period of time is required for charging the voltage V_{BL} of the bit line to a predetermined value.

[0016]

According to the conventional MRAM reading method, it is required to charge the bit line to the target voltage Vt whenever the information is read, and the required time (charge time) tc is one of the factors to delay the reading operation.

[0017]

The present invention has been contrived to solve such problems of the prior art, and an object thereof is to provide an MRAM capable of reading information at high speed and a method for driving the MRAM.

[0018]

[Means for Solving the Problems]

In order to achieve the above object, according to the present invention, means as described below well be disclosed.

[0019]

A magnetic memory of the present invention comprises:

a plurality of variable resistors arrayed as memory elements in a matrix;

a plurality of bit lines each of which is arranged on each row of the matrix and connected to one terminal of each variable resistors belonging to the same row;

a read circuit which detects resistance values of the variable resistors based on currents flowing through the bit lines; and

a load element arranged on the bit lines independently of the memory elements.

[0020]

According to an embodiment of the present invention, the load element is to suppress a fluctuation of a load of the bit line.

[0021]

According to the present invention, since a fluctuation of a load of the bit line is suppressed by the load resistor, the time for setting a voltage for the bit line is reduced for each selection of a variable resistor.

[0022]

According to an embodiment of the present invention, the load element includes a resistor having the same structure as a structure of the variable resistor, a resistor having a structure different from the structure of the variable resistor, a current source, a diode, or a combination of the resistor, the current source, and the diode.

[0023]

According to an embodiment of the present invention, each variable resistor includes a tunneling magnetoresistive element.

[0024]

According to an embodiment of the present invention, the tunneling magnetoresistive element is magnetized mainly perpendicular to a film surface.

[0025]

According to another embodiment of the present invention, the tunneling magnetoresistive element is magnetized mainly parallel to a film surface.

[0026]

According to an embodiment of the present invention, the memory further comprises a plurality of switches for selecting the variable resistors in correspondence with the variable resistors.

[0027]

According to an embodiment of the present invention, each switch includes a field effect type transistor, a bipolar transistor, a thin film transistor, a diode, or a combination of the field effect type transistor, the bipolar transistor, the thin film transistor, and the diode.

[0028]

A ferromagnetic memory driving method of the present invention is a driving method for driving a ferromagnet memory comprising a plurality of variable resistors arrayed as memory elements in a matrix, a plurality of bit lines each of which is arranged on each row of the matrix and connected to one terminal of each variable resistors belonging to the same row, a read circuit which detects resistance values of said variable resistors based on currents flowing through said bit lines, and a load element arranged on said bit lines independently of said memory elements, which method comprising the steps of:

selecting the variable resistors connected to the same bit line continuously so as to apply a predetermined voltage to the variable resistors; and

detecting information written in the variable resistors based on currents flowing through the variable resistors.

[0029]

According to an embodiment of the present invention, the driving method comprises the steps of: selecting the variable resistors connected to the same bit line continuously and suppressing variations in the voltages of the bit lines including the variable resistors when applying a predetermined voltage to the variable resistors.

[0030]

According to an embodiment of the present invention, the step of suppressing variations in the voltages of the bit lines is a step of always turning on one of the plurality of switches connected to the same bit line.

[0031]

According to the present invention, the variable resistors connected to the same bit line are continuously selected in such a manner that at least one variable resistor is selected without fail so that the information thereof is read. As a result, the time for setting a voltage for the bit line for each selection of a variable resistor is not required.

[0032]

A ferromagnetic memory driving method according to another embodiment of the present invention is a method for driving a nonvolatile memory which comprises a plurality of variable resistors arranged in a matrix, a plurality of switches respectively corresponding to the variable resistors, and a plurality of bit lines arranged on each row of the matrix, one terminal of each variable resistor being connected to the same bit line and the other terminal of the variable resistor being connected to one terminal of each corresponding switch,

the driving method comprising the steps of:

suppressing variations in the voltages of the bit line including the variable resistors to apply a predetermined voltage to the variable resistor; and detecting information written in the variable resistors based on currents flowing through the variable resistors.

[0033]

According to an embodiment of the present invention, the step of suppressing variations in the voltages of the bit lines is a step of always turning on one of the plurality of switches connected to the same bit line.

[0034]

A ferromagnetic memory driving method according to still another embodiment of the present invention is a method for driving a ferromagnetic memory which comprises a plurality of variable resistors arranged in a matrix and capable of selecting an electric resistance by selecting a direction of magnetization of a ferromagnet, a plurality of switches respectively corresponding to the variable resistors, and a plurality of bit lines arranged on each row of the matrix, one terminal of each variable resistor being connected to the same bit line and the other terminal of the variable resistor being connected to one terminal of each corresponding switch,

the driving method comprising the step of:

selecting two or more of the plurality of variable resistors connected to the same bit line continuously so as to always select at least one of the variable resistors connected to the same bit line when reading information.

[0035]

[Detailed Description of the Preferred Embodiments]

The present invention provides a method for driving a ferromagnetic memory having a plurality of variable resistors. The variable resistor used in the present invention can select a resistance value by selecting the magnetization direction of a ferromagnet.

[0036]

The magnetoresistive element of this variable resistor is a tunneling magnetoresistive element (MTJ; Magnetic Tunnel Junction, TMR; Tunneling MagnetoResistive element) having a structure in which a tunneling insulating film is sandwiched between two ferromagnetic layers. This element has recently received attention because it can increase the magnetoresistance ratio.

[0037]

A variable resistor having two ferromagnetic layers, like a TMR element, exhibits a low resistance value when the magnetization direction of one ferromagnetic layer coincides with that of the other ferromagnetic layer (to be referred to as "parallel" hereinafter). The variable resistor exhibits a high resistance value when the magnetization directions of the two layers are opposite to each other (to be referred to as "antiparallel" hereinafter). The TMR element can record and maintain information (magnetization information) expressing two states by the difference in magnetization direction. This type of variable resistor can be utilized as the memory cell of a nonvolatile memory.

[0038]

In a ferromagnetic memory as a nonvolatile memory using a variable resistor, memory cells are arrayed in a matrix on a substrate. In the ferromagnetic memory, parallel or antiparallel magnetization information is recorded (written) in a ferromagnet functioning as a recording layer in a memory cell at an arbitrary position. For this purpose, a plurality of crossing wires are laid out so as to pass through the vicinity of variable resistors. A write current flows through a pair of crossing wires (write and bit lines) to induce a magnetic field which intensifies near the intersection. Magnetization information is written in a corresponding variable resistor.

[0039]

In reading out written magnetization information from a ferromagnetic memory, a memory cell is selected from memory cells arrayed on a substrate, and whether the magnetization state of the variable resistor of the memory cell is parallel or antiparallel must be output (read out).

[0040]

For this purpose, e.g., bit lines run in the row direction of the matrix in the ferromagnetic memory. One terminal of each of the variable resistors of memory cells belonging to one row are connected to a bit line on this row. Further, a selection switch is disposed between the other terminal of the variable resistor and ground.

[0041]

The bit lines and selection switches are controlled, and the target voltage Vt is applied across each variable resistor to flow a current through the variable resistor. From the resistance value, whether the state of the variable resistor is parallel or antiparallel is read out as magnetization information.

[0042]

The present invention provides a ferromagnetic memory for suppressing variations in the voltage level of a bit line or suppressing variations in burden including a variable resistor connected to a bit line before the start of read operation or during read operation when a plurality of variable resistors on the same bit line are sequentially, successively selected to read out signals from the variable resistors.

[0043]

As means of suppressing variations in voltage level, such a driving method as sequentially, successively selecting a plurality of variable resistors on the same bit line during read operation so as to always select any one of the variable resistors is employed. As far as at least one of variable resistors on the same bit line is always selected, the burden of the bit line is determined by the resistance value of the variable resistor, and variations in voltage level can be suppressed.

[0044]

By using this means, variations in the voltage level of the bit line are suppressed, and the voltage level of the bit line during read operation is maintained at the target voltage Vt. A magnetic memory in which the time taken to charge the bit line to the target voltage Vt is shortened.

[0045]

Preferred embodiments of the present invention will be described in detail with reference to the accompanying drawings.

[0046]

Fig. 1 is a circuit diagram showing the arrangement of a ferromagnetic memory according to the first embodiment of the present invention.

[0047]

A ferromagnetic memory of the first embodiment comprises field effect type transistors (FET) T11, T12, T13, T21, T22, T23, T31, T32, and T33, TMR elements R11, R12, R13, R21, R22, R23, R31, R32, write lines WL1, WL2, and WL3, bit lines BL1, BL2, and BL3, memory cell selection lines SL1, SL2, and SL3, field effect type transistors Ts1, Ts2, and Ts3, a read circuit 90. The read circuit 90 comprises a load resistor Rr, a field effect type transistor Tr, voltage sources Vb and Vref, and a sense amplifier SA.

[0048]

The bit lines BL1, BL2, and BL3 run parallel to each other. The write lines WL1, WL2, and WL3 also run parallel to each other. The bit lines BL1, BL2, and BL3 and the write lines WL1, WL2, and WL3 cross each other. The memory cell selection lines SL1, SL2, and SL3 and the write lines run parallel to each other. The memory cell selection lines SL1, SL2, and SL3 run parallel to each other and to the write lines WL1, WL2, and WL3.

[0049]

The field effect type transistors T11, T12, T13, T21, T22, T23, T31, T32, and T33 are paired with the corresponding TMR elements R11, R12, R13, R21, R22, R23, R31, R32, and R33 to constitute memory cells. The nine memory cells are arrayed in a 3 × 3 matrix at the intersections of the bit lines BL1, BL2, and BL3, the write lines WL1, WL2, and WL3, and the memory cell selection lines.

[0050]

The drain of each of the field effect type transistors T11, T12, T13, T21, T22, T23, T31, T32, and T33 is connected to one terminal of each of the paired TMR elements R11, R12, R13, R21, R22, R23, R31, R32, and R33. The source of each of the field effect type transistors T11, T12, T13, T21, T22, T23, T31, T32, and T33 is grounded. The other terminal of each of the TMR elements R11, R12, and R13 is connected to the bit line BL1. Similarly, the other terminal of each of the TMR elements R21, R22, and R23 is connected to the bit line BL2. The other terminal of each of the TMR elements R31, R32, and R33 is connected to the bit line BL3. The gates of the field effect type transistors T11, T21, and T31 are connected to the memory cell selection line SL1. Similarly, the gates of the field effect type transistors T12, T22, and T32 are connected to the memory cell selection line SL2. The gates of the field effect type transistors T13, T23, and T33 are connected to the memory cell selection line SL3.

[0051]

The bit line BL1 is connected to the source of the field effect type transistor Ts1; the bit line BL2, to that of the field effect type transistor Ts2; and the bit line BL3, to that of the field effect type transistor Ts3.

[0052]

The drains of the field effect type transistors Ts1, Ts2, and Ts3 are commonly connected to the source of the field effect type transistor Tb. One terminal of the load resistor Rr is pulled up to the power supply voltage, and its other terminal is connected to the drain of the field effect type transistor Tb and one input terminal of the sense amplifier SA. The gate of the field effect type transistor Tb receives a voltage from the voltage source Vb. The other input terminal of the sense amplifier SA receives a voltage from the voltage source Vref.

[0053]

The field effect type transistors T11, T21, and T31 are switches for selecting the corresponding TMR elements

R11, R21, and R31. If the memory cell selection line SL1 is selected, the field effect type transistors T11, T21, and T31 are turned on to ground one terminal of each of the TMR elements R11, R21, and R31.

[0054]

Similarly, if the memory cell selection line SL2 is selected, one terminal of each of the TMR elements R12, R22, and R32 is grounded. If the memory cell selection line SL3 is selected, one terminal of each of the TMR elements R13, R23, and R33 is grounded.

[0055]

When the field effect type transistors Ts1, Ts2, and Ts3 are selected, they supply the target voltage Vt to the bit lines BL1, BL2, and BL3.

[0056]

For example, to select the TMR element R11, the field effect type transistor Ts1 and field effect type transistor T11 are turned on to supply the target voltage Vt to the bit line BL1. A voltage almost equal to the target voltage Vt is applied across the TMR element R11, and a signal current corresponding to the resistance value of the TMR element R11 is output to the read circuit 90.

[0057]

The field effect type transistor Tb constitutes a gate ground circuit using a TMR element as a load. The field effect type transistor Tb supplies a voltage (target voltage Vt) corresponding to the bias voltage Vb to a bit line, and outputs the obtained signal current from the drain to the load resistor Rr.

[0058]

The load resistor Rr converts a signal current input from the drain of the field effect type transistor Tb into a voltage.

[0059]

The sense amplifier SA compares the input voltage levels of the two input terminals, and outputs information "1" or "0" on the basis of the comparison result. In the first embodiment, a signal voltage read out using the load resistor Rr is compared with the reference voltage Vref.

[0060]

Information is written in the ferromagnetic memory of the first embodiment by flowing currents to both a desired bit line and write line. Information is read out from the ferromagnetic memory of the first embodiment by turning on the field effect type transistor (e.g., Ts1 or Ts2) of a bit line to be selected, and comparing a readout signal voltage with the reference voltage Vref by the sense amplifier SA. At this time, the reference voltage may be a predetermined voltage supplied from the voltage source, as shown in Fig. 1, a voltage generated by a reference voltage generation dummy cell, or a voltage obtained by reversing the state of a cell subjected to read operation.

[0061]

Fig. 2 represents schematic views showing the structure of a TMR element adopted in the first embodiment of the present invention. In general, a ferromagnet internally generates polarization (magnetization) M upon application of the external magnetic field H in a direction in which magnetization easily occurs (easy axis of magnetization). The relationship between the magnetization M and the external magnetic field H draws a hysteresis curve, as shown in Fig. 3. An external magnetic field at a boundary where the magnetization is switched, i.e., an external magnetic field where the M-H curve crosses the H axis is called a coercive force Hc.

[0062]

The ferromagnet has a property that the coercive force Hc becomes smaller upon application of both an external magnetic field along the easy axis of magnetization and an external magnetic field in a direction different from the easy axis of magnetic field than upon application of a single external magnetic field along the easy axis of magnetization. In this case, the magnetization of the ferromagnet is switched by an external magnetic field weaker than the original coercive force Hc.

[0063]

As shown in Fig. 2, the TMR element has the two ferromagnetic layers 16 serving as a large-coercive-force hard layer and small-coercive-force soft layer, and the tunneling insulating film 17. In the TMR element, the tunneling insulating film 17 is sandwiched between the two ferromagnetic layers 16. The TMR element exhibits a different resistance value depending on whether the magnetization directions of the hard and soft layers are the same direction (parallel) or opposite directions (antiparallel). This phenomenon is a so-called magnetoresistance effect. The variation width of the resistance value is 40% or more at maximum.

[0064]

In Fig. 2, (a) shows a TMR element in which the ferromagnetic layer is magnetized parallel to the film surface (longitudinal magnetization type). In Fig. 2, (b) shows a TMR element in which the ferromagnetic layer is magnetized perpendicular to the film surface (perpendicular magnetization type). In either case, the magnetization of the ferromagnetic layer is switched by a magnetic field induced by a current flowing through a wire.

[0065]

A TMR element whose magnetization is to be switched receives an external magnetic field along the easy axis of magnetization that is induced by a current flowing through a write line, and an external magnetic field in a direction different from the easy axis of magnetization that is induced by a current flowing through a bit line.

[0066]

In many cases, the ferromagnetic layers 16 functioning as the hard and soft layers of the TMR element are made of, e.g., a metal material or alloy. The tunneling insulating film 17 is made of an oxide insulating material such as Al_2O_3. The resistance value of the TMR element is high when the magnetizations of the hard and soft layers are antiparallel, and low when they are parallel to each other.

[0067]

Fig. 4 is a schematic sectional view showing a cell structure of a longitudinal magnetization memory cell according to the first embodiment of the present invention.

[0068]

In the longitudinal magnetization memory cell shown in Fig. 4, on a p-type semiconductor substrate 1, there is formed a field effect type transistor which is constituted by n-type diffusion regions 2 and 3, a gate insulating film 4, and a gate electrode 5. This field effect type transistor is isolated by a region isolation area 15.

[0069]

One terminal of the TMR element 12 serving as a variable resistor capable of selecting a resistance value by selecting the magnetization direction of a ferromagnet is connected to the n-type diffusion region 3 via the local wire 10 and contact plug 6. The other terminal of the TMR element 12 is coupled to the bit line 13.

[0070]

The n-type diffusion region 2 is connected to the ground wire 8 via the contact plug 7.

[0071]

The write line 9 crosses the bit line 13.

[0072]

In write operation, currents flow through the write line 9 and bit line 13, and an external magnetic field induced by the currents changes the magnetization direction of the ferromagnet of the TMR element 12.

[0073]

As shown in Fig. 4, in the longitudinal magnetization memory cell, the write line 9 is arranged below the TMR element 12 so as to induce a magnetic field parallel to the film surface of the TMR element 12 by a write current.

[0074]

Fig. 5 is a schematic sectional view showing a cell structure of a perpendicular magnetization memory cell according to a second embodiment of the present invention.

[0075]

As shown in Fig. 5, in the perpendicular magnetization memory cell, the write line 9 is arranged beside the TMR element 12 so as to induce a magnetic field almost perpendicular to the film surface of the TMR element 12 by a write current.

[0076]

Read operation of the ferromagnetic memory of the second embodiment will be described by exemplifying a 3 × 3-bit ferromagnetic memory shown in Fig. 1. In this case, an operation of successively reading out pieces of information from the TMR elements R11, R12, and R13 will be explained.

[0077]

First, the field effect type transistor Ts1 is turned on to select the bit line BL1. The field effect type transistor T11 is turned on by the memory cell selection line SL1 to apply a voltage (target voltage Vt) corresponding to the bias voltage Vb across the TMR element R11. The voltage of the bit line BL1 is indefinite before the field effect type transistor Ts1 is turned on. A predetermined time is taken to, e.g., charge the bit line BL1 until the voltage reaches the target voltage Vt.

[0078]

Then, a signal current flowing through the TMR element R11 is transferred to the read circuit 90 via the field effect type transistor Ts1. The signal current is converted into a voltage by the load resistor Rr, and the voltage is input to one input terminal of the sense amplifier SA. The sense amplifier SA compares the voltage input to one input terminal with the reference voltage Vref of the other input terminal, and outputs information "0" or "1".

[0079]

After that, the field effect type transistor T11 is turned off, and the field effect type transistor T12 is turned on. At this time, the field effect type transistor

Ts1 is kept on, and the bit line BL1 is kept selected.

[0080]

One of the TMR elements R11, R12, and R13 connected to the bit line BL1 is kept selected, and the voltage of the bit line BL1 is maintained at the target voltage Vt without greatly changing the load of the bit line BL1. Thus, the time required to set the voltage of the bit line BL1 to the target voltage Vt can be eliminated in turning on the field effect type transistor T12 and selecting the TMR element R12. Immediately when the field effect type transistor T12 is turned on, a signal current flowing through the TMR element R12 can be transferred to the read circuit 90 via the field effect type transistor Ts1.

[0081]

Then, the field effect type transistor T12 is turned off, and the field effect type transistor T13 is turned on. Also in this case, the voltage of the bit line BL1 is maintained at the target voltage Vt. A signal current flowing through the TMR element R13 can be immediately transferred to the read circuit 90 via the field effect type transistor Ts1.

[0082]

According to the ferromagnetic memory read method of the first embodiment, TMR elements are successively selected to always select one of TMR elements connected to the same bit line, and information in the TMR element is read out. The time required to set the voltage of the bit line is not required every selection of a TMR element, and high-speed read operation can be realized.

[0083]

As described above, the ferromagnetic memory of the first embodiment can realize, by a simple structure and driving method, an object which cannot have been achieved by a conventional memory.

[0084]

In the present embodiment, the field effect type transistor is employed as a switching element. However, the switching element may be a bipolar transistor, a thin film transistor, a diode, or a combination of them.

[0085]

Next, a specific example of the ferromagnetic memory of the first embodiment will be described below.

(First Example)

A circuit configuration of a ferromagnetic memory of a first example will be described below with reference to Fig. 6.

[0086]

The ferromagnetic memory of the first example shown in Fig. 6 has the same structure as that shown in Fig. 1, and comprises nine memory cells arranged in a 3 x 3 matrix, write lines WL1, WL2 and WL3, bit lines BL1, BL2 and BL3, memory cell selection lines SL1, SL2 and SL3, field effect type transistors Ts1, Ts2, Ts3, and a read circuit 90. The read circuit 90 comprises a load resistor Rr, a field effect type transistor Tr, voltage sources Vb and Vref, and a sense amplifier SA.

[0087]

Each memory cell is comprised of one field effect type transistor (FET) T11, T12, T13, T21, T22, T23, T31, T32 or T33 corresponding to its position on the 3 x 3 matrix and one TMR element R11, R12, R13, R21, R22, R23, R31, R32 or R33 corresponding thereto. The field effect type transistors Ts1, Ts2 and Ts3 are respectively disposed between each of the bit lines BL1, BL2 and BL3 and the read circuit 90.

[0088]

An operation for reading out the information of the TMR elements R11, R12 and R13 continuously will be described in the following.

[0089]

In the first example, pieces of information "1", "0", and "1" are written in the TMR elements R11, R12, and R13. The memory cell selection lines SL1, SL2, and SL3 operate such that one of them is always sequentially selected.

[0090]

First, the field effect type transistor Ts1 is turned on to select the bit line BL1. The memory cell selection line SL1 is turned on to apply a voltage (target voltage Vt) corresponding to the bias voltage Vb across the TMR element R11. At this time, a signal current I1 flows through the read circuit 90.

[0091]

Then, the field effect type transistor T11 is turned off, and the field effect type transistor T12 is turned on. At this time, a signal current I2 flows through the read circuit 90.

[0092]

Finally, the field effect type transistor T12 is turned off, and the field effect type transistor T13 is turned on. At this time, a signal current I3 flows through the read circuit 90.

[0093]

Since "1", "0", and "1" are respectively written in the TMR elements R11, R12, and R13, the current values of the signal currents I1, I2, and I3 satisfy $I1 = I3 < I2$.

[0094]

Fig. 7 is a timing chart showing changes in a voltage V_{BL1} of the bit line BL1, the signal current Isig, a load R_{BL1} viewed from the bit line in the above-described read operation.

[0095]

The operation of the first example will be further explained with reference to Fig. 7.

[0096]

At least one of memory cells on the same bit line is always selected during read operation of successively reading out pieces of information from memory cells connected to the same bit line. The variation amount of the load of the bit line is determined by only a change in resistance value caused by the MR ratio of the TMR element. Thus, the voltage of the bit line is kept almost constant. As is apparent from Fig. 7, this operation does not require any period for charging the bit line, and a current as a result of reading out information is output at high speed.

[0097]

A second embodiment of the present invention will be described.

[0098]

The second embodiment of the present invention is characterized in that a dummy load serving as a load element for suppressing variations in burden before the start of read or during read operation is connected to a bit line as a means for suppressing variations in burden. The load of a selected bit line is either a synthetic load of a dummy load and variable resistor or a single dummy load, and thus variations in burden can be suppressed.

[0099]

By using this means and successively reading out pieces of information from TMR elements connected to the same bit line, variations in the burden of the bit line are suppressed, and the voltage level of the bit line during read operation is maintained at the target voltage Vt. The time required to charge the bit line up to the target voltage Vt is shortened.

[0100]

Note that the second embodiment assumes a resistor as a dummy load. Instead, the dummy load may be a resistor having the same structure as that of the variable resistor, a resistor having a structure different from that of the variable resistor, a current source, a diode, or a combination of them.

[0101]

Next, a specific example of the ferromagnetic memory of the second embodiment will be described below.

(Second Example)

A circuit configuration of a ferromagnetic memory of a second example will be described below with reference to Fig. 8.

[0102]

The second example is different from the first example in that the dummy loads Rd1, Rd2 and Rd3 are connected between the bit lines BL1, BL2 and BL3 and the ground points. An operation of the second example is different from that of the first example in that memory cell selection lines SL1, SL2, and SL3 are successively selected at a predetermined interval and in that no memory cell selection line is turned on during read from each memory cell.

[0103]

First, a field effect type transistor Ts1 is turned on to select a bit line BL1. A field effect type transistor

T11 is turned on to apply a voltage (target voltage Vt) corresponding to the bias voltage Vb across a TMR element R11. A signal current flowing through a read circuit 90 at this time is a synthetic current of a signal current flowing through the TMR element R11 and a signal current Id flowing through the dummy load Rd1.

[0104]

Then, the field effect type transistor T11 is turned off. A signal current flowing through the read circuit 90 at this time is only the signal current Id flowing through the dummy load Rd1.

[0105]

In this manner, a signal current when the field effect type transistor T11, T12, or T13 is ON is a synthetic current of the signal current I4, I5, or I6 flowing through the corresponding TMR element R11, R12, or R13 and the signal current Id flowing through the dummy load Rd1. A signal current when no field effect type transistor T11, T12, or T13 is ON is only the signal current Id flowing through the dummy load Rd1.

[0106]

Fig. 9 is a timing chart showing changes in the voltage V_{BL1} of the bit line BL1, the signal current Isig, the load R_{BL1} viewed from the bit line in the above-described read operation.

[0107]

A more detailed operation of the second example will be explained with reference to Fig. 9.

[0108]

In the second example, since the dummy load Rd1 is connected to the bit line, variations in the load of the bit line BL1 are suppressed by the dummy load Rd1 even if no memory cell is selected in read operation of successively reading out pieces of information from memory cells connected to the same bit line. As is apparent from Fig. 9, the voltage of the bit line BL1 is kept almost constant, and a time (charge time) tc required to charge the bit line is shortened. Accordingly, a current as a result of reading out information is output at high speed.

[0109]

Note that the first and second embodiments of the present invention can be more effectively combined.

[0110]

[Effect of the Invention]

As has been described above, the load element suppresses variations in the load of the bit line, and the time taken to set the voltage of the bit line every selection of the variable resistor can be shortened, realizing high-speed read operation.

[0111]

Since the variable resistors connected to the same bit line are continuously selected in such a manner that at least one variable resistor is inevitably selected, and the information thereof is read out, the time for setting the voltage of the bit line is not required whenever a variable resistor is selected, thereby realizing high-speed read operation.

[Brief Description of the Drawings]

[Figure 1]

A circuit diagram showing the arrangement of a ferromagnetic memory according to the first embodiment of the present invention.

[Figure 2]

Schematic views showing the structure of a TMR element according to the first embodiment, in which (a) shows a TMR element of the longitudinal magnetization type and (b) shows that of the perpendicular magnetization type.

[Figure 3]

A graph showing the magnetization characteristic of a magnetic substance.

[Figure 4]

A sectional view showing an example of a cell structure of a perpendicular magnetization memory cell according to the first embodiment of the present invention.

[Figure 5]

A sectional view showing an example of a cell structure of a longitudinal magnetization memory cell according to the first embodiment of the present invention.

[Figure 6]

A circuit diagram showing a ferromagnetic memory according to the first example.

[Figure 7]

A timing chart showing changes in a voltage V_{BL1} of the bit line BL1, the signal current Isig, a load R_{BL1} viewed from the bit line in the first example.

[Figure 8]

A circuit diagram showing a ferromagnetic memory according to the second example.

[Figure 9]

A timing chart showing changes in a voltage V_{BL1} of the bit line BL1, the signal current Isig, a load R_{BL1} viewed from the bit line in the second example.

[Figure 10]

A circuit diagram for explaining read operation of a conventional MRAM.

[Figure 11]

A graph showing a signal current Isig - target voltage Vt characteristic for explaining a target voltage Vt in the circuit diagram shown in Fig. 10.

[Figure 12]

A timing chart for explaining an operation when pieces of information are successively read out from arbitrary memory cells by a conventional method.

[Description of Reference Numerals or Symbols]

1 … p-type semiconductor substrate

2, 3 … n-type diffusion regions

4 … gate insulating film

5 … gate electrode

6 … contact plug
7 … contact plug
8 … ground wire
9 … write line
10 … local wire
11 … lower electrode
12 … TMR element
13 … bit line
14 … protective insulating film
15 … region isolation area
16 … ferromagnetic layers
17 … tunneling insulating film
90 … read circuit
R11 to R14, R21 to R24, R31 to R34 … TMR elements
T11 to T13, T21 to T23, T31 to T33, Tb1 to Tb3, Ts1 to Ts3 … field effect type transistors
SA … sense amplifier
Rd1 to Rd3 … dummy loads
Rr … load resistor
Tb … field effect type transistor
Vb, Vref … voltage sources
BL1 to BL3 … bit lines
SL1 to SL3 … sense amplifier selection lines
WL1 to WL3 … write lines
I1 to I3 … signal currents
Id … signal current
tc … charge time

[Name of the Document] Abstract]

[Abstract]

[Object]

An object of the present invention is to provide a ferromagnetic memory capable of reading information and a method for driving the same.

[Means for Achieving the Object]

A plurality of variable resistors R are capable of selecting electric resistance values based on a direction of magnetization of a ferromagnet and are arrayed in a matrix. Bit lines BL are arranged on each row of the matrix to be parallel to each other and are connected to one terminal the variable resistors R belonging to the same row. A read circuit 90 detects the resistance values of the variable resistors R based on currents flowing through the bit lines BL. Load elements Rd suppress fluctuations in the load of the bit lines BL. Switches T are connected between the variable resistors R and the ground point, respectively, in order to select the variable resistors R. The variable resistors R which are connected to the same bit line are sequentially and continuously selected in such a manner that at least one of the switches T connected to the variable resistor R connected to the bit line is always turned on, whereby a predetermined voltage is applied to the resistor to detect magnetization information based on the currents flowing through the variable resistors.

[Elected Drawing]

Figure 8

Applicant's Information

Identification No. [000001007]

1. Date of Change: August 30, 1990

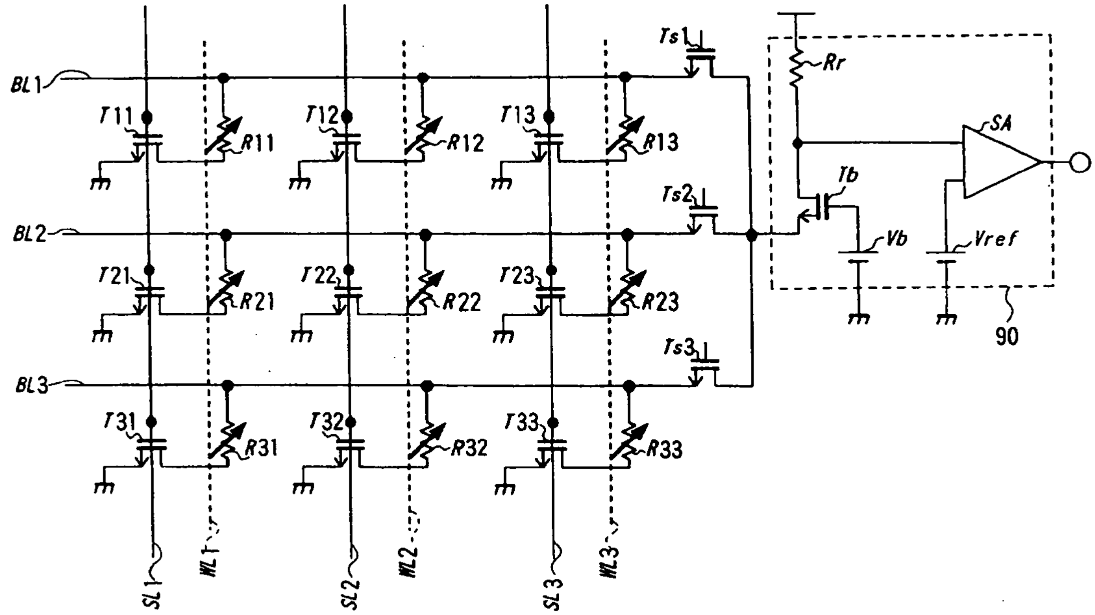
(Reason of Change) New Registration

Address: 3-30-2, Shimomaruko, Ohta-ku, Tokyo

Name: CANON KABUSHIKI KAISHA

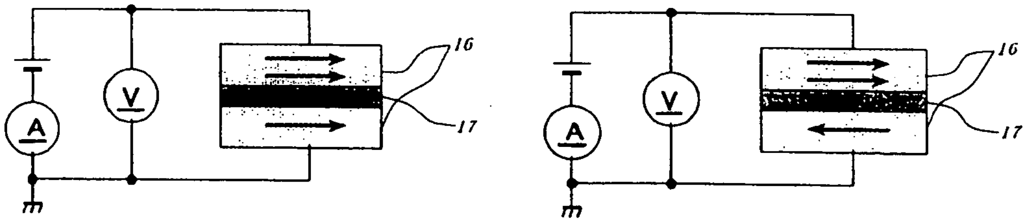
【書類名】　図面　[Name of the Document] Drawings

【図１】　Fig. 1

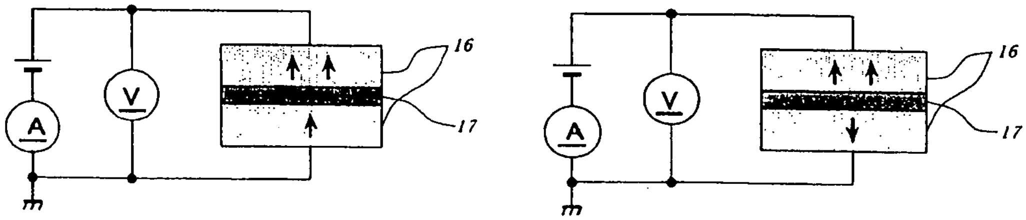


【図２】　Fig. 2

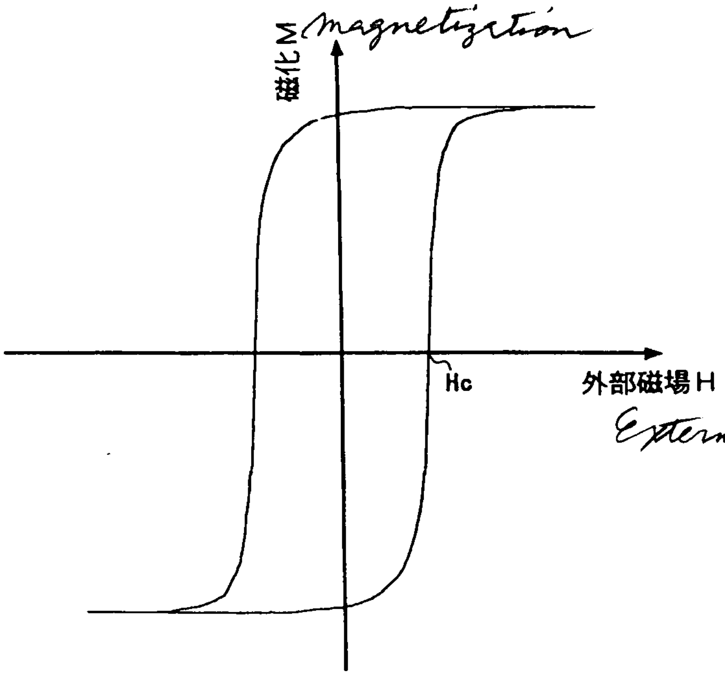
（a）



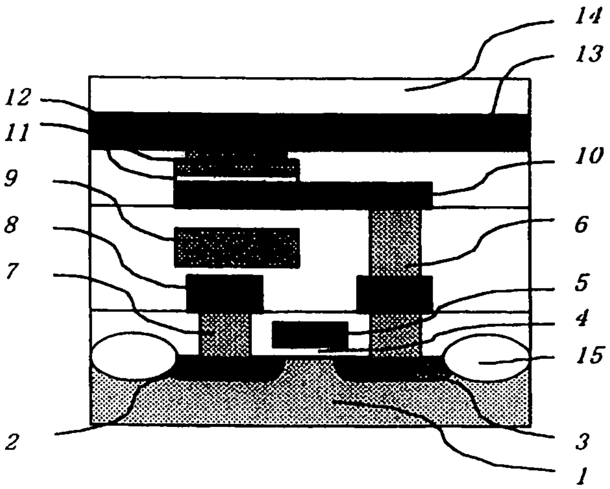
（b）



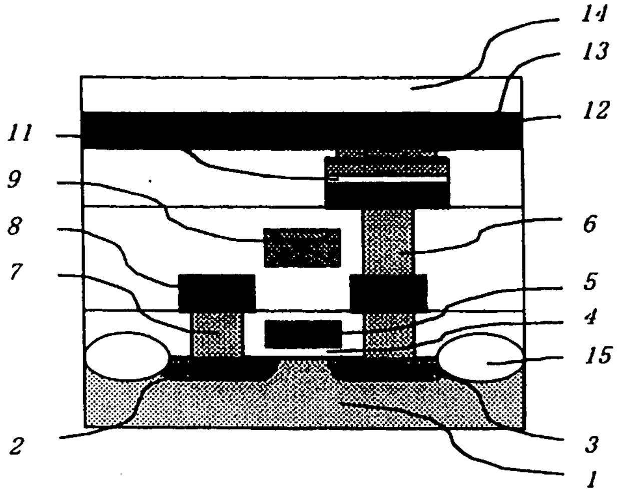
【図３】 Fig.3



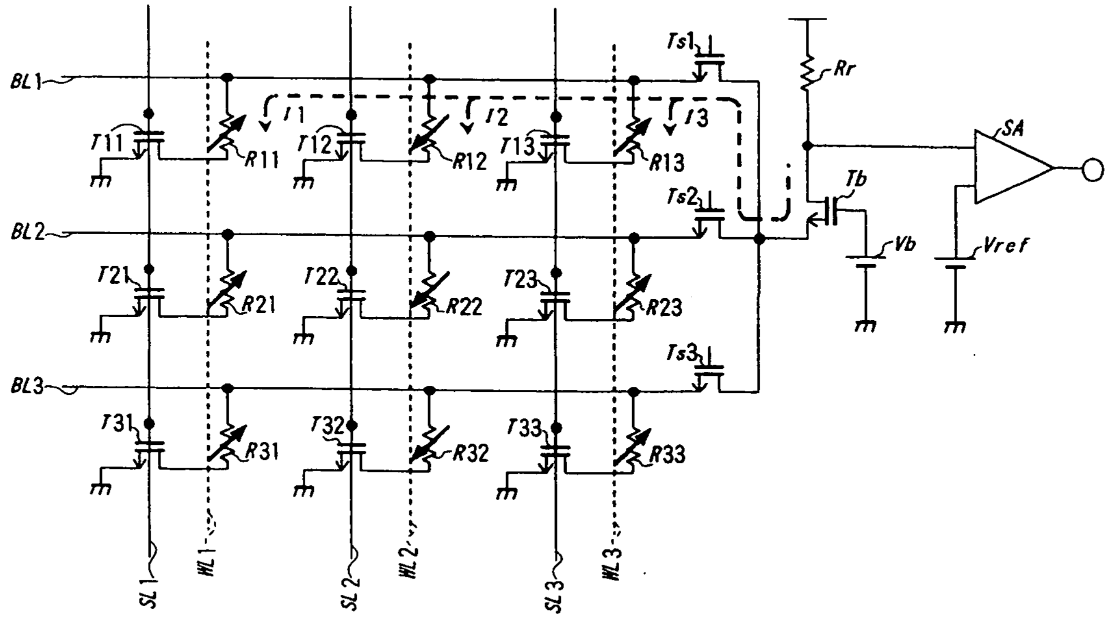
【図４】 Fig.4



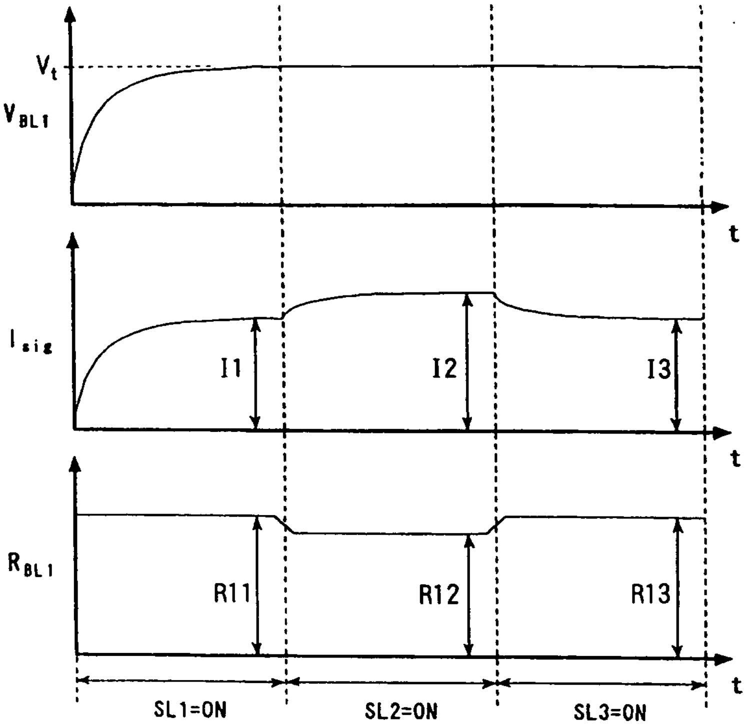
【図５】 Fig. 5



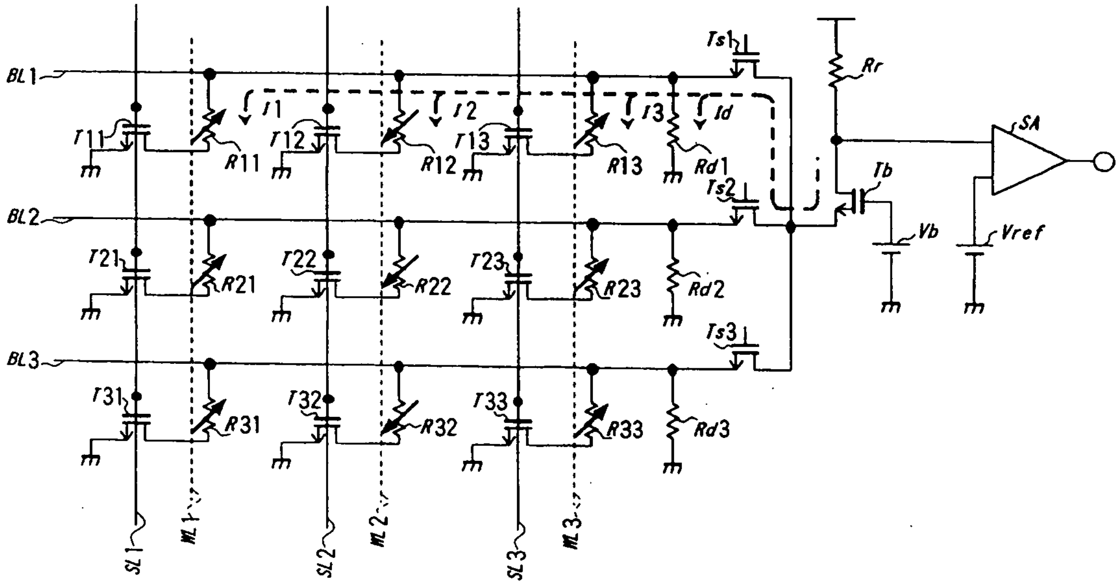
【図６】 Fig. 6



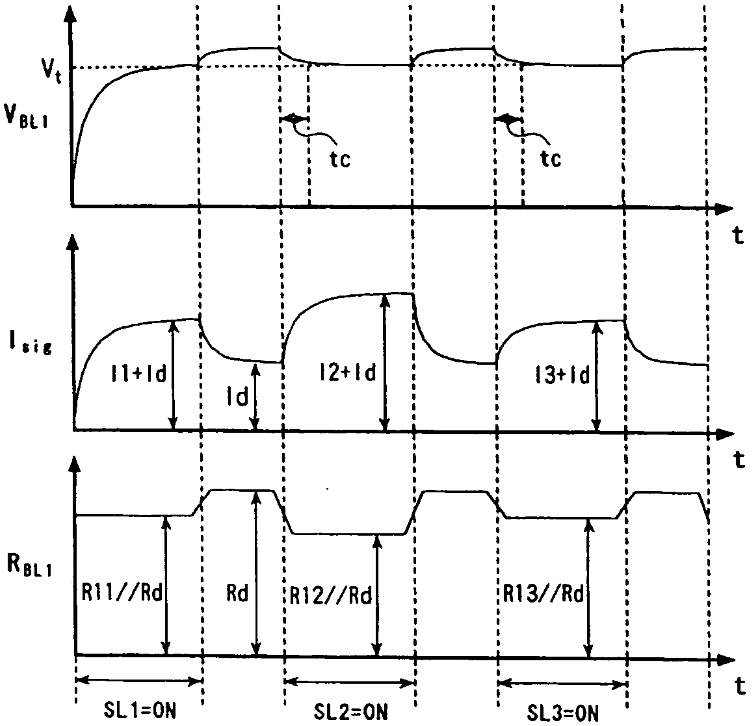
【図７】 Fig. 7



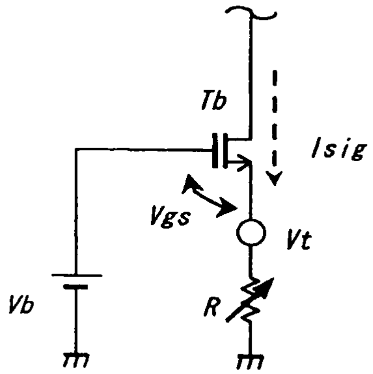
【図８】 Fig. 8



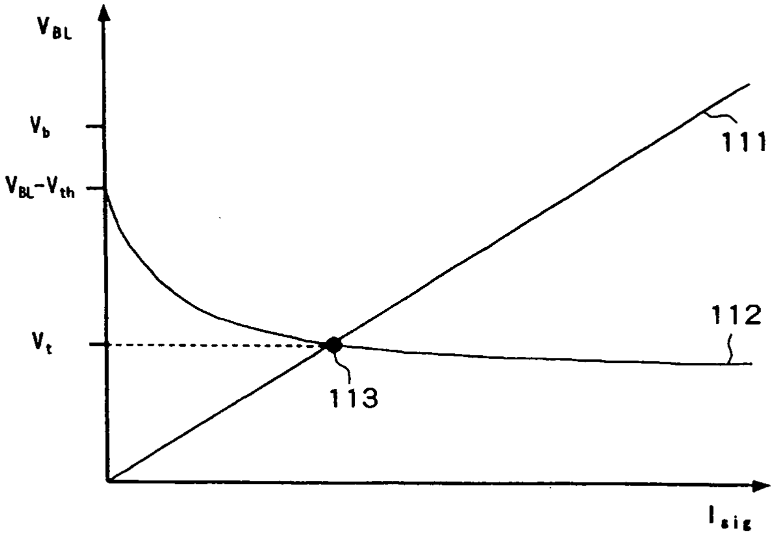
【図９】 Fig. 9



【図１０】 Fig. 10



【図１１】 Fig. 11



【図１２】 Fig. 12